WHAT IS CLAIMED IS:

1. An array substrate for an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line to define a pixel region having an aperture area;

a thin film transistor disposed at one corner of the pixel region and connected to the gate line and the data line, the thin film transistor including a semiconductor layer;

a common line spaced apart from the gate line and substantially parallel to the gate line;

a common electrode extending from the common line and including a plurality of common electrode patterns, wherein an outermost portion of common electrode pattern is substantially rectangle-shaped within the pixel region and has a substantially circular opening in the middle thereof;

a capacitor electrode overlapping the substantially rectangle shaped common electrode pattern, the capacitor electrode connected to the thin film transistor;

a pixel connecting line disposed substantially parallel to the data line in the pixel region and connected to the capacitor electrode; and

a pixel electrode disposed within the substantially circular opening, extending from the pixel connecting line and including a plurality of pixel electrode patterns,

wherein an innermost pixel electrode pattern has a substantially circular shape and other pixel electrode are patterned to have circular bands,

wherein an innermost portion of the plurality of common electrodes is circular band shaped, and

wherein the aperture area is circular band shaped.

2. The array substrate of claim 1, wherein the plurality of common electrode patterns are arranged in an alternating pattern with the plurality of pixel electrode patterns.

3. The array substrate of claim 1, wherein the innermost portion of the common electrode pattern is disposed at a center portion of the pixel region where the common line and the pixel connecting line cross.

4. The array substrate of claim 1, wherein the capacitor electrode includes first and second capacitor electrode patterns that overlap bottom and top portions of the outermost common electrode pattern, respectively.

5. The array substrate of claim 4, wherein the first capacitor electrode pattern is connected to the thin film transistor.

6. The array substrate of claim 4, wherein the first and second capacitor electrode patterns have rounded sides, respectively, which face each other.

7. The array substrate of claim 1, wherein the pixel region has a substantially square shape.

8. The array substrate of claim 1, wherein four neighboring pixel regions correspond to red, green, blue and white colors, respectively.

9. The array substrate of claim 1, wherein the capacitor electrode and the common electrode overlap to form a first storage capacitor.

10. The array substrate of claim 9, wherein the capacitor electrode overlaps a previous gate line of a previous neighboring pixel region to form a second storage capacitor.

11. The array substrate of claim 1, wherein the pixel and common electrode patterns are disposed within the substantially circular opening except the outermost portion of the common electrode pattern.

12. The array substrate of claim 1, further comprising a semiconductor line located under the data line and having the same pattern shape as the data line, wherein the semiconductor layer extends from the semiconductor line.

13. A method of forming an array substrate for an in-plane switching liquid crystal display device, comprising:

forming a gate line having a gate electrode, a common electrode including a plurality of common electrode patterns and a common line disposed substantially parallel to and spaced apart from the gate line on a substrate using a first mask process, wherein an outermost portion of the common electrode pattern has a substantially rectangle shape and a substantially circular opening in the middle thereof;

forming a gate insulating layer on the gate line, the common electrode and the common line;

forming a semiconductor layer on the gate insulating layer and over the gate electrode using a second mask process;

forming a data line that crosses the gate line to define a pixel region having an aperture area, a source electrode extending from the data line, and a drain electrode spaced apart from the source electrode using a third mask process, wherein the source and drain electrodes overlap opposite end portions of the semiconductor layer, the semiconductor layer being exposed between the source and drain electrodes, and the gate electrode, the semiconductor layer, the source electrode and the drain electrode forming a thin film transistor;

forming a passivation layer over an entire surface of the substrate to cover the thin film transistor and patterning the passivation layer using a fourth mask process to form a drain contact hole to expose a portion of the drain electrode; and

forming a capacitor electrode that overlaps the outermost portion of the common electrode pattern and connects to the drain electrode, a pixel connecting line connected to the capacitor electrode, and a pixel electrode extending from the pixel connecting line and including a plurality of pixel electrode patterns on the passivation layer using a fifth mask process,

wherein an innermost pixel electrode pattern has a substantially circular shape,

wherein an innermost portion of the plurality of common electrode patterns and the plurality of pixel electrode patterns are circular band shaped, and

wherein the aperture area is circular band shaped.

14. The method of claim 13, wherein the plurality of common electrode patterns are arranged in an alternating pattern with the plurality of pixel electrode patterns.

15. The method of claim 13, wherein the innermost portion of common electrode pattern is disposed at a center portion of the pixel region where the common line and the pixel connecting line cross.

16. The method of claim 13, wherein the capacitor electrode includes first and second capacitor electrode patterns that overlap bottom and top portions of the outermost common electrode pattern, respectively.

17. The method of claim 16, wherein the first capacitor electrode pattern is connected to the thin film transistor.

18. The method of claim 16, wherein the first and second capacitor electrode patterns have rounded sides, respectively, that face each other.

19. The method of claim 13, wherein the pixel region has a substantially square shape.

20. The method of claim 13, wherein four neighboring pixel regions correspond to red, green, blue and white colors, respectively.

21. The method of claim 13, wherein the capacitor electrode and the common electrode overlap to form a first storage capacitor.

22. The method of claim 21, wherein the capacitor electrode overlaps a previous gate line of a previous neighboring pixel region to form a second storage capacitor.

23. The method of claim 13, wherein the pixel and common electrode patterns are disposed within the substantially circular opening except the outermost portion of the common electrode pattern.

24. A method of forming an array substrate for an in-plane switching liquid crystal display device, comprising:

forming a gate line having a gate electrode, a common electrode including a plurality of common electrode patterns and a common line disposed substantially parallel to and spaced apart from the gate line on a substrate using a first mask process, wherein an outermost portion of the common electrode pattern is substantially rectangle-shaped and has a substantially circular opening in the middle thereof;

forming a gate insulating layer on the gate line, the common electrode and the common line;

forming a data line that crosses the gate line to define a pixel region having an aperture area, a source electrode that extends from the data line, a drain electrode spaced apart from the source electrode across the gate electrode, a semiconductor layer under the data line and having the same pattern shape as the data line, a semiconductor layer that extends from the semiconductor line over the gate electrode and under the source and drain electrodes using a second mask process, wherein the source and drain electrodes overlap opposite end portions of the gate electrode, the semiconductor layer being exposed between the source and drain electrodes, and the gate electrode, the semiconductor layer, the source electrode and the drain electrode form a thin film transistor;

forming a passivation layer over an entire surface of the substrate to cover the thin film transistor and patterning the passivation layer using a third mask process to form a drain contact hole to expose a portion of the drain electrode; and

forming a capacitor electrode that overlaps the outermost portion of the common electrode pattern and connects to the drain electrode, a pixel connecting line connected to the capacitor electrode, and a pixel electrode that extends from the pixel connecting line and includes a plurality of pixel electrode patterns on the passivation layer using a fourth mask process,

wherein an innermost pixel electrode pattern has a substantially circular shape,

wherein an innermost portion of the plurality of common electrode patterns and the plurality of pixel electrode patterns are circular band shaped, and

wherein the aperture area is circular band shaped.

25. The method of claim 24, wherein the plurality of common electrode patterns are arranged in an alternating pattern with the plurality of pixel electrode patterns.

26. The method of claim 24, wherein the innermost portions of the common electrode pattern is disposed at a center portion of the pixel region where the common line and the pixel connecting line cross.

27. The method of claim 24, wherein the capacitor electrode includes first and second capacitor electrode patterns that overlap bottom and top portions of the outermost common electrode pattern, respectively.

28. The method of claim 27, wherein the first capacitor electrode pattern is connected to the thin film transistor.

29. The method of claim 27, wherein the first and second capacitor electrode patterns have rounded sides, respectively, that face each other.

30. The method of claim 24, wherein the pixel region has a substantially square shape.

31. The method of claim 24, wherein four neighboring pixel regions correspond to red, green, blue and white colors, respectively.

32. The method of claim 24, wherein the capacitor electrode and the common electrode overlap to form a first storage capacitor.

33. The method of claim 32, wherein the capacitor electrode overlaps a previous gate line of a previous neighboring pixel region to form a second storage capacitor.

34. The method of claim 24, wherein the pixel and common electrode patterns are disposed within the substantially circular opening, except the outermost portion of the common electrode pattern.

35. An array substrate for use in an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line to define a pixel region having an aperture area;

a thin film transistor disposed at one corner of the pixel region and connected to the gate line and the data line, the thin film transistor including a semiconductor layer;

a common electrode disposed in the pixel region and having first and second common electrode patterns, wherein the first common electrode pattern is substantially rectangle-shaped and has a substantially circular opening in the middle thereof, and the second common electrode pattern is disposed in the substantially circular opening and has a substantially gyre shape;

a common line substantially perpendicular to and crossing the data line and connecting the common electrode to a neighboring common electrode in a neighboring pixel region;

a capacitor electrode overlapping the first common electrode pattern, the capacitor electrode connected to the thin film transistor; and

a pixel electrode disposed within the substantially circular opening and having a substantially gyre shape along a side of the second common electrode pattern,

wherein the pixel electrode and the second common electrode pattern each have the substantially gyre shape,

wherein the aperture area is substantially gyre shaped.

36. The array substrate of claim 35, wherein the second common electrode pattern extends from the first common electrode pattern.

37. The array substrate of claim 36, wherein the pixel electrode extends from the capacitor electrode, the extension of the pixel electrode starting next to the extension of the second common electrode pattern.

38. The array substrate of claim 35, wherein a first helical turn of the pixel electrode is located between the first common electrode pattern and a first helical turn of the second common electrode pattern.

39. The array substrate of claim 35, wherein the common line is formed as one unitary pattern with the common electrode.

40. The array substrate of claim 35, wherein the capacitor electrode has a substantially rounded side along the substantially circular opening of the first common electrode pattern.

41. The array substrate of claim 35, wherein four neighboring pixel regions correspond to red, green, blue and white colors, respectively.

42. The array substrate of claim 35, wherein the capacitor electrode and the common electrode overlap to form a first storage capacitor.

43. The array substrate of claim 42, wherein the capacitor electrode overlaps a previous gate line of a previously neighboring pixel region to form a second storage capacitor.

44. The array substrate of claim 35, further comprising a semiconductor line under the data line and having the same pattern shape as the data line, wherein the semiconductor layer extends from the semiconductor line.

45. A method of forming an array substrate for an in-plane switching liquid crystal display device, comprising:

forming a gate line having a gate electrode, a common electrode having first and second common electrode patterns, and a common line substantially parallel to and spaced apart from the gate line on a substrate using a first mask process, wherein the first common electrode pattern is substantially rectangle-shaped and has a substantially circular opening in the middle thereof, and the second common electrode pattern is disposed in the substantially circular opening and has a substantially gyre shape;

forming a gate insulating layer on the gate line, the common electrode and the common line;

forming a semiconductor layer on the gate insulating layer and over the gate electrode using a second mask process;

forming a data line that crosses the gate line to define a pixel region having an aperture area, a source electrode extending from the data line, and a drain electrode spaced apart from the source electrode using a third mask process, wherein the source and drain electrodes overlap opposite end portions of the semiconductor layer, the semiconductor layer being exposed between the source and drain electrodes, and the gate electrode, the semiconductor layer, the source electrode and the drain electrode forming a thin film transistor;

forming a passivation layer over an entire surface of the substrate to cover the thin film transistor and patterning the passivation layer using a fourth mask process to form a drain contact hole to expose a portion of the drain electrode; and

forming a capacitor electrode overlapping the first common electrode pattern, and a pixel electrode within the substantially circular opening and having a substantially gyre shape along a side of the second common electrode pattern using a fifth mask process,

wherein the capacitor electrode is connected to the thin film transistor, and the pixel electrode and the second common electrode pattern each have the substantially gyre shape,

wherein the aperture area is substantially gyre shaped.

46. The method of claim 45, wherein the second common electrode pattern extends from the first common electrode pattern.

47. The method of claim 46, wherein the pixel electrode extends from the capacitor electrode, the extension of the pixel electrode starting next to the extension of the second common electrode pattern.

48. The method of claim 45, wherein a first helical turn of the pixel electrode is disposed between the first common electrode pattern and a first helical turn of the second common electrode pattern.

49. The method of claim 45, wherein the common line is formed as one unitary pattern with the common electrode.

50. The method of claim 45, wherein the capacitor electrode has a substantially rounded side along the substantially circular opening of the first common electrode pattern.

51. The method of claim 45, wherein four neighboring pixel regions correspond to red, green, blue and white colors, respectively.

52. The method of claim 45, wherein the capacitor electrode and the common electrode overlap to form a first storage capacitor.

53. The method of claim 52, wherein the capacitor electrode overlaps a previous gate line of a previously neighboring pixel region to form a second storage capacitor.

54. A method of forming an array substrate for an in-plane switching liquid crystal display device, comprising:

forming a gate line having a gate electrode, a common electrode having first and second common electrode patterns, and a common line substantially parallel to and spaced apart from the gate line on a substrate using a first mask process, wherein the first common electrode pattern is substantially rectangle-shaped and has a substantially circular opening in the middle thereof, and the second common electrode pattern is disposed in the substantially circular opening and has a substantially gyre shape;

forming a gate insulating layer on the gate line, the common electrode and the common line;

forming a data line that crosses the gate line to define a pixel region having an aperture area, a source electrode extending from the data line, a drain electrode spaced apart from the source electrode across the gate electrode, a semiconductor layer under the data line and having the same pattern shape as the data line, and a semiconductor layer extending from the semiconductor line over the gate electrode and under the source and drain electrode using a second mask process, wherein the source and drain electrodes overlap opposite end portions of the gate electrode, the semiconductor layer being exposed between the source and drain electrodes, and the gate electrode, the semiconductor layer, the source electrode and the drain electrode forming a thin film transistor;

forming a passivation layer over an entire surface of the substrate to cover the thin film transistor and patterning the passivation layer using a third mask process to form a drain contact hole to expose a portion of the drain electrode; and

forming a capacitor electrode that overlaps the first common electrode pattern, and a pixel electrode disposed within the substantially circular opening and having a substantially gyre shape along the second common electrode pattern using a fourth mask process, wherein the capacitor electrode is connected to the thin film transistor, and the pixel electrode and the second common electrode pattern each have the substantially gyre shape, wherein the aperture area is substantially gyre shaped.

55. The method of claim 54, wherein the second common electrode pattern extends from the first common electrode pattern.

56. The method of claim 55, wherein the pixel electrode extends from the capacitor electrode, the extension of the pixel electrode starting next to the extension of the second common electrode pattern.

57. The method of claim 54, wherein a first helical turn of the pixel electrode is disposed between the first common electrode pattern and a first helical turn of the second common electrode pattern.

58. The method of claim 54, wherein the common line is formed as one unitary pattern with the common electrode.

59. The method of claim 54, wherein the capacitor electrode has a substantially rounded side along the substantially circular opening of the first common electrode pattern.

60. The method of claim 54, wherein four neighboring pixel regions correspond to red, green, blue and white colors, respectively.

61. The method of claim 54, wherein the capacitor electrode and the common electrode overlap to form a first storage capacitor.

62. The method of claim 61, wherein the capacitor electrode overlaps a previous gate line of a previously neighboring pixel region to form a second storage capacitor.

63. An array substrate for an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line to define a pixel region having an aperture area;

a semiconductor line under the data line and having the same pattern shape as the data line;

a thin film transistor disposed at one corner of the pixel region and connected to the gate and data lines, the thin film transistor including source and drain electrodes and a semiconductor layer extending from the semiconductor line;

a common line spaced apart from and substantially parallel to the gate line;

a common electrode extending from the common line and including a plurality of common electrode patterns, wherein an outermost common electrode pattern is substantially rectangle-shaped within the pixel region and has a substantially circular opening in the middle thereof;

a capacitor electrode overlapping a previous gate line of a previously neighboring pixel region;

a pixel electrode within the substantially circular opening and including a plurality of pixel electrode patterns; and

a pixel connecting line substantially parallel to the data line in the pixel region and connected to the capacitor electrode, the pixel electrode and the drain electrode of the thin film transistor,

wherein the pixel electrode overlaps portions of the pixel connecting line and directly contacts the pixel connecting line,

wherein an innermost pixel electrode pattern has a substantially circular shape and other pixel electrode patterns are patterned to have circular bands, and

wherein an innermost portion of the plurality of common electrode patterns is substantially circular band shaped, and

wherein the aperture area is circular band shaped.

64. The array substrate of claim 63, wherein the plurality of common electrode patterns are arranged in an alternating pattern with the plurality of pixel electrode patterns.

65. The array substrate of claim 63, wherein the innermost portion of the common electrode pattern is disposed at a center portion of the pixel region where the common line and the pixel connecting line cross.

66. The array substrate of claim 63, wherein the capacitor electrode pattern is connected to the thin film transistor though the pixel connecting line.

67. The array substrate of claim 63, wherein four neighboring pixel regions correspond to red, green, blue and white colors, respectively.

68. The array substrate of claim 63, wherein the capacitor electrode overlaps the outermost common electrode pattern and forms a first storage capacitor with the overlapped portion of the outermost common electrode pattern, and the capacitor electrode overlaps the previous gate line to form a second storage capacitor.

69. The array substrate of claim 63, wherein the pixel and common electrode patterns are disposed within the substantially circular opening, except the outermost common electrode pattern.

70. A method of forming an array substrate for use in an in-plane switching liquid crystal display device, comprising:

forming a gate line having a gate electrode, a common electrode including a plurality of common electrode patterns, and a common line substantially parallel to and spaced apart from the gate line on a substrate using a first mask process, wherein an outermost common

electrode pattern is substantially rectangle-shaped and has a substantially circular opening in the middle thereof;

forming a gate insulating layer on the gate line, the common electrode and the common line;

forming a data line that crosses the gate line to define a pixel region having an aperture area, a source electrode extending from the data line, a drain electrode spaced apart from the source electrode across the gate electrode, a pixel connecting line extending from the drain electrode and substantially parallel to the data line, a capacitor electrode over a previous gate line with extending from the pixel connecting line, a semiconductor line under the data line and having the same pattern shape with the data line, and a semiconductor layer extending from the semiconductor line over the gate electrode and under the source and drain electrodes using a second mask process, wherein the source and drain electrodes overlap opposite end portions of the gate electrode, the semiconductor layer being exposed between the source and drain electrodes, and the gate electrode, the semiconductor layer, the source electrode and the drain electrode form a thin film transistor;

forming a photoresist pattern on the thin film transistor using a third mask process, the photoresist pattern having openings between the plurality of common electrode patterns;

forming a transparent conductive layer on an entire surface of the substrate to cover the photoresist pattern; and

removing the transparent conductive layer on the photoresist pattern by stripping the photoresist pattern to obtain a pixel electrode, wherein the pixel electrode fits in the openings of the photoresist and directly contacts the pixel connecting line, the pixel electrode including a plurality of pixel electrode patterns,

wherein an innermost pixel electrode pattern has a substantially circular shape and other pixel electrode patterns are patterned to have circular bands,

wherein an innermost portion of the plurality of common electrode patterns is substantially circular band shaped, and

wherein the aperture area is circular band shaped.

71. The method of claim 70, wherein the plurality of common electrode patterns are arranged in an alternating pattern with the plurality of pixel electrode patterns.

72. The method of claim 70, wherein the innermost common electrode pattern is disposed at a center portion of the pixel region where the common line and the pixel connecting line cross.

73. The method of claim 70, wherein the capacitor electrode pattern is connected to the thin film transistor though the pixel connecting line.

74. The method of claim 70, wherein four neighboring pixel regions correspond to red, green, blue and white colors, respectively.

75. The method of claim 70, wherein the capacitor electrode overlaps the outermost common electrode pattern and forms a first storage capacitor with the overlapped portion of the outermost common electrode pattern, and the capacitor electrode overlaps the previous gate line to form a second storage capacitor.

76. The method of claim 70, wherein the pixel and common electrode patterns are within the substantially circular opening except the outermost common electrode pattern.

77. An array substrate for use in an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line to define a pixel region having an aperture area;

a semiconductor line under the data line and having the same pattern shape as the data line;

a thin film transistor disposed at one corner of the pixel region and connected to the gate and data lines, the thin film transistor including source and drain electrodes and a semiconductor layer extending from the semiconductor line;

a common line spaced apart from and substantially parallel to the gate line;

a capacitor electrode overlapping a previous gate line of a previously neighboring pixel region;

a pixel connecting line substantially parallel to the data line within the pixel region and connected to the capacitor electrode and the drain electrode of the thin film transistor;

a common electrode including a plurality of common electrode patterns, each of the common electrode patterns divided into two parts by the pixel connecting line without overlapping the pixel connecting line; and

a pixel electrode within a substantially circular opening and including a plurality of pixel electrode patterns without overlapping the common line,

wherein an outermost common electrode pattern is substantially rectangle-shaped within the pixel region and has a substantially circular opening in the middle thereof, and other common electrode patterns are shaped substantially like semicircular arcs,

wherein an innermost pixel electrode pattern has a substantially rod shape and is disposed within an area of pixel connecting line, and other pixel electrode patterns have a substantially semicircular-arc shape, and

wherein the plurality of common electrode patterns and the plurality of pixel electrode patterns form substantially circular band shaped aperture areas.

78. The array substrate of claim 77, wherein the pixel electrode overlaps portions of the pixel connecting line and directly contacts the pixel connecting line.

79. The array substrate of claim 77, wherein the common electrode overlaps portions of the common line and directly contacts the common line.

80. A method of forming an array substrate for use in an in-plane switching liquid crystal display device, comprising:

forming a gate line having a gate electrode and a common line substantially parallel to and spaced apart from the gate line on a substrate using a first mask process;

forming a gate insulating layer on the gate line and the common line;

forming a data line that crosses the gate line to define a pixel region having an aperture area, a source electrode extending from the data line, a drain electrode spaced apart from the source electrode, a pixel connecting line extending from the drain electrode and substantially parallel to the data line, a capacitor electrode over a previous gate line extending from the pixel connecting line, a semiconductor line under the data line and having the same pattern shape as the data line, and a semiconductor layer extending from the semiconductor line over the gate electrode and under the source and drain electrode using a second mask process, wherein the source and drain electrodes overlap opposite end portions of the gate electrode, the semiconductor layer being exposed between the source and drain electrodes, and the gate electrode, the semiconductor layer, the source electrode and the drain electrode form a thin film transistor;

forming a photoresist pattern on the thin film transistor using a third mask process, the photoresist pattern including two first symmetric open portions separated from the pixel connecting line without overlapping the pixel connecting line and two second symmetric open portions separated from the common line without overlapping the common line;

etching the gate insulating layer using the photoresist pattern as an etch mask to expose the common and pixel connecting lines under the two first symmetric open portions;

forming a transparent conductive layer on an entire surface of the substrate having the photoresist pattern; and

removing the transparent conductive layer on the photoresist pattern by stripping the photoresist pattern to obtain a common electrode and a pixel electrode, wherein the common and pixel electrodes fit in the first and second symmetric open portions of the photoresist, the common electrode including a plurality of common electrode patterns, and the pixel electrode including a plurality of pixel electrode patterns,

wherein an outermost common electrode pattern is substantially rectangle-shaped within the pixel region and has a substantially circular opening in the middle thereof, and other common electrode patterns are patterned to have substantially semicircular arcs,

wherein an innermost pixel electrode pattern has a substantially rod shape and is disposed within an area of the pixel connecting line, and the other pixel electrode patterns are substantially semicircular-arc shaped, and

wherein the aperture area is circular band shaped.

81. The method of claim 80, wherein the pixel electrode overlaps portions of the pixel connecting line and directly contacts the pixel connecting line;

82. The method of claim 80, wherein the common electrode overlaps portions of the common line and directly contacts the common line.

83. An array substrate for use in an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line to define a pixel region having an aperture region;

a thin film transistor disposed at one corner of the pixel region and connected to the gate line and the data line, the thin film transistor including a gate electrode, a semiconductor layer and source and drain electrodes;

a common line spaced apart and substantially parallel to the gate line;

a common electrode extending from the common line and including a plurality of common electrode patterns, wherein an outermost common electrode pattern is substantially shaped like a rectangle within the pixel region and has a substantially rectangular opening in the middle thereof;

a capacitor electrode overlapping the substantially rectangular common electrode pattern, the capacitor electrode connected to the thin film transistor;

a pixel connecting line substantially parallel to the data line in the pixel region and connected to the capacitor electrode; and

a pixel electrode within the substantially rectangular opening, extending from the pixel connecting line and including a plurality of pixel electrode patterns,

wherein an innermost pixel electrode pattern has a substantially circular shape and other pixel electrode patterns are patterned to have circular bands,

wherein an innermost portion of the plurality of common electrode patterns is circular band shaped, and the aperture area is circular band shaped.

84. The array substrate of claim 83, wherein the plurality of common electrode patterns are arranged in an alternating pattern with the plurality of pixel electrode patterns.

85. The array substrate of claim 83, wherein the innermost portion of the common electrode pattern is disposed at a center portion of the pixel region where the common line and the pixel connecting line cross.

86. The array substrate of claim 83, wherein the capacitor electrode includes first and second capacitor electrode patterns that overlap bottom and top portions of the outermost common electrode pattern, respectively.

87. The array substrate of claim 86, wherein the first capacitor electrode pattern is connected to the thin film transistor.

88. The array substrate of claim 83, wherein four neighboring pixel regions correspond to red, green, blue and white colors, respectively.

89. The array substrate of claim 83, wherein the capacitor electrode and the common electrode overlap to form a first storage capacitor.

90. The array substrate of claim 89, wherein the capacitor electrode overlaps a previous gate line of a previous neighboring pixel region to form a second storage capacitor.

91. An array substrate of claim 83, wherein the pixel and common electrode patterns are disposed within the substantially rectangular opening except the outermost common electrode pattern.

92. An array substrate for use in an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line to define a pixel region having aperture regions;

a semiconductor line under the data line and having a same patterned shape as the data line;

a thin film transistor disposed at one corner of the pixel region and connected to the gate and data lines, the thin film transistor including source, gate electrode, and drain electrodes and a semiconductor layer extending from the semiconductor line;

a common line spaced apart from and substantially parallel to the gate line;

a capacitor electrode overlapping a previous gate line of a previously neighboring pixel region;

a pixel connecting line substantially parallel to the data line in the pixel region, extending from the drain electrode, and connecting the capacitor electrode and the drain electrode of the thin film transistor;

a passivation layer over the thin capacitor and pixel electrodes, the passivation layer having first and second contact holes that expose the common line and pixel connecting line, respectively;

a common electrode on the passivation layer and having a plurality of common electrode patterns, wherein an outermost common electrode pattern is continuously connected to neighboring outermost common electrode patterns of neighboring pixel regions and has a substantially circular opening in the middle of the pixel region, and other common electrode patterns have circular band shapes; and

a pixel electrode disposing within the substantially circular opening and including a plurality of pixel electrode patterns, wherein an innermost pixel electrode pattern has a substantially circular shape and is disposed over a crossing of the common and pixel connecting lines, and the other pixel electrode patterns have circular band shapes.

93. The array substrate of claim 92, wherein the common electrode overlaps the common line and pixel connecting lines and only contacts the common line through the first contact holes.

94. The array substrate of claim 92, wherein the pixel electrode overlaps the common and pixel connecting lines and only contacts the pixel connecting line through the second contact holes.

95. The array substrate of claim 92, wherein the plurality of common electrode patterns are arranged in an alternating pattern with the plurality of pixel electrode patterns.

96. The array substrate of claim 92, wherein the innermost common electrode pattern is disposed at a center portion of the pixel region.

97. The array substrate of claim 92, wherein four neighboring pixel regions correspond to red, green, blue and white colors, respectively.

98. The array substrate of claim 92, wherein the common electrode and the pixel electrode are formed of ITO.

99. The array substrate of claim 92, wherein the common electrode is over the data line.

100. A method of forming an array substrate for an in-plane switching liquid crystal display device, comprising:

forming a gate line having a gate electrode, and a common line substantially parallel to and spaced apart from the gate line on a substrate using a first mask process,

forming the gate insulating layer on the gate line, common electrode and the common line;

forming a data line that crosses the gate line to define a pixel region having an aperture region, a source electrode that extends from the data line, a drain electrode spaced apart from the source electrode, a semiconductor layer under the data line having the same patterned as the data line, a thin film transistor located at one corner of the pixel region and connected to the gate and data lines, a capacitor electrode overlapping a previous gate line of a neighboring pixel region, a pixel connecting line substantially parallel to the data line in the pixel region and extending form the drain electrode using a second mask process, wherein the pixel connecting line connects the capacitor electrode and the drain electrode of the thin film transistor;

forming a passivation layer having first and second contact holes that expose the common line and the pixel connecting line in a third mask process;

forming a common electrode on the passivation layer, the common electrode having a plurality of common electrode patterns, wherein an outermost common electrode is continuously connected to neighboring outermost common electrode patterns and having a

substantially circular opening in the middle of the pixel region, and an inner common electrode patterns having a circular band shape;

forming a pixel electrode within the substantially circular opening and including a plurality of pixel electrode patterns, wherein an innermost pixel electrode pattern has a substantially circular shape and is disposed over a crossing of the common and pixel connecting lines and inner pixel electrode patterns having a circular band shape,

wherein the common electrode and the pixel electrode are patterned using a fourth mask process.

101. The method according to claim 100, wherein the common electrode and the pixel electrode are formed of ITO.

102. The method according to claim 100, wherein the common electrode is over the data line.

103. An array substrate for an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line to define a pixel region having an aperture area;

a gate pad connected to one end of the gate line;

a data pad connected to one end of the data line;

a gate pad terminal connected to the gate pad;

a data pad terminal connected to the data pad;

a semiconductor line under the data line and having the same pattern shape as the data line;

a thin film transistor disposed at one corner of the pixel region and connected to the gate and data lines, the thin film transistor including source and drain electrodes and a semiconductor layer extending from the semiconductor line;

a common line spaced apart from and substantially parallel to the gate line;

a common electrode extending from the common line and including a plurality of common electrode patterns, wherein an outermost common electrode pattern is substantially rectangle-shaped within the pixel region and has a substantially circular opening in the middle thereof;

a capacitor electrode overlapping a previous gate line of a previously neighboring pixel region;

a pixel electrode within the substantially circular opening and including a plurality of pixel electrode patterns; and

a pixel connecting line substantially parallel to the data line in the pixel region and connected to the capacitor electrode, the pixel electrode and the drain electrode of the thin film transistor,

wherein the innermost pixel electrode pattern is shaped like a rod and disposed within an area of the pixel connecting line,

wherein the pixel electrode overlaps portions of the pixel connecting line and directly contacts the pixel connecting line,

wherein other pixel electrode patterns are patterned to have semicircular shapes, and

wherein the semiconductor line extends underneath the source and drain electrodes, the pixel connection line and the capacitor electrode,

wherein an innermost portion of the plurality of common electrode patterns is substantially circular band shaped, and

wherein the aperture area is circular band shaped.

104. The array substrate of claim 103, wherein the plurality of common electrode patterns are arranged in an alternating pattern with the plurality of pixel electrode patterns.

105. The array substrate of claim 103, wherein the innermost portion of the pixel electrode pattern is disposed at a center portion of the pixel region where the common line and the pixel connecting line cross.

106. The array substrate of claim 103, wherein the capacitor electrode pattern is connected to the thin film transistor though the pixel connecting line.

107. The array substrate of claim 103, wherein four neighboring pixel regions correspond to red, green, blue and white colors, respectively.

108. The array substrate of claim 103, wherein the pixel and common electrode patterns are disposed within the substantially circular opening, except the outermost common electrode pattern.

109. A method of forming an array substrate for use in an in-plane switching liquid crystal display device, comprising:

forming a gate line having a gate electrode, a common electrode including a plurality of common electrode patterns, a gate pad connected to one end of the gate line and a common line substantially parallel to and spaced apart from the gate line on a substrate using a first mask process, wherein an outermost common electrode pattern is substantially rectangle-shaped and has a substantially circular opening in the middle thereof;

forming a gate insulating layer on the gate line, the common electrode, the gate pad and the common line;

forming a data line that crosses the gate line to define a pixel region having an aperture area, a source electrode extending from the data line, a drain electrode spaced apart from the source electrode across the gate electrode, a pixel connecting line extending from the drain electrode and substantially parallel to the data line, a capacitor electrode over a previous gate line with extending from the pixel connecting line, a data pad connected to one end of the data line, a semiconductor line under the data line and having the same pattern shape with the data line, and a semiconductor layer extending from the semiconductor line over the gate electrode and under the source and drain electrodes and pixel connecting line and capacitor electrode using a second mask process, wherein the source and drain electrodes overlap opposite end portions of the gate electrode, the semiconductor layer being exposed between the source and drain electrodes, and the gate electrode, the semiconductor layer, the source electrode and the drain electrode form a thin film transistor;

forming a passivation layer over the data line, the source and drain electrodes, the data pad, the pixel connecting line, and the capacitor electrode;

forming a photoresist pattern on the passivation layer to cover the thin film transistor using a third mask process, the photoresist pattern having openings between the plurality of common electrode patterns and contact openings exposing the gate and data pads;

forming a transparent conductive layer on an entire surface of the substrate to cover the photoresist pattern; and

removing the transparent conductive layer on the photoresist pattern by stripping the photoresist pattern to obtain a pixel electrode, a gate pad terminal and a data pad termianl, wherein the pixel electrode fits in the openings of the photoresist and directly contacts the pixel connecting line, the pixel electrode including a plurality of pixel electrode patterns,

wherein an innermost pixel electrode pattern has a substantially rod shape and other pixel electrode patterns are patterned to have semicircular shapes,

wherein an innermost portion of the plurality of common electrode patterns is substantially circular band shaped, and

wherein the aperture area is circular band shaped.

110. The method of claim 109, wherein the plurality of common electrode patterns are arranged in an alternating pattern with the plurality of pixel electrode patterns.

111. The method of claim 109, wherein the innermost pixel electrode pattern is disposed at a center portion of the pixel region where the common line and the pixel connecting line cross.

112. The method of claim 109, wherein the capacitor electrode pattern is connected to the thin film transistor though the pixel connecting line.

113. The method of claim 109, wherein the capacitor electrode overlaps the outermost common electrode pattern and forms a storage capacitor with the overlapped portion of the outermost common electrode pattern.

114. The method of claim 109, wherein the pixel and common electrode patterns are within the substantially circular opening except the outermost common electrode pattern.